



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,576	06/15/2005	Marko Van Houdt	NL021302	9022

65913 7590 08/22/2008  
NXP, B.V.  
NXP INTELLECTUAL PROPERTY DEPARTMENT  
M/S41-SJ  
1109 MCKAY DRIVE  
SAN JOSE, CA 95131

EXAMINER
----------

PERILLA, JASON M

ART UNIT	PAPER NUMBER
----------	--------------

2611

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

08/22/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/538,576	<b>Applicant(s)</b> VAN HOUDT ET AL.	
	<b>Examiner</b> JASON M. PERILLA	<b>Art Unit</b> 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. Claims 1-15 are pending in the instant application.

#### ***Response to Amendment/Argument***

2. The Applicants remarks, filed June 24, 2008, have been considered in view of the amendments to the claims.

In view of the amendments to the claims, modified rejections are made below.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-14 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Buckland (U.S. Pat. No. 4744081).

Regarding claim 1, Buckland discloses a frame synchronizing (abstract) device for a binary data transmission system wherein digital data are transmitted as a serial bit stream (fig. 1, ref. 24) organized into frames (col. 1, lines 5-15; see also fig. 3), each frame including a pre-defined frameheader (i.e. "frame word"; col. 1, lines 20-25), comprising: a serial input (fig. 1, ref. 24) parallel output (fig. 1, "m") shift register (fig. 1, refs. 16 and 18) for receiving said serial bit stream (fig. 1, "SERIAL DATA") and outputting said frames (fig. 1, "PARALLEL DATA") in a consecutive order, said shift register (fig. 1, refs. 16 and 18) including a serial input portion (fig. 1, ref. 16) and a parallel output portion (fig. 1, "m", ref. 18) and having at least m stages ("m-bit words";

Art Unit: 2611

col. 2, line 65) as the number of bits in a frame (see discussion below), first clock circuitry (inherent, but not illustrated; generates "SERIAL CLOCK" 25) that generates first clock pulses, separated by a first time period (i.e. "one pulse" period; col. 3, line 31), for clocking the serial input portion (fig. 1, ref. 16) of the shift register; second clock circuitry (fig. 1, ref. 20) that generates second clock pulses (fig. 1, "CLOCK") for clocking the parallel output portion (fig. 1, ref. 18) of the shift register, the second clock circuitry generating the second clock pulses responsive to the first clock pulses, and controlling circuitry (*inter alia*, fig. 1, refs. 20, 22, 14, and 12) for detecting (fig. 1, ref. 14) whether or not a frameheader or "frame word" (fig. 1, "FRAME WORD") is present at the output of said parallel output portion and, if not, controlling (fig. 1, ref. 10; "SLIP") said shift register so that the clocking of the parallel output portion is delayed by at least the first time period (i.e. "one pulse" period; col. 3, line 31, the control circuitry delaying the clocking of the parallel output portion (col. 3, lines 33-39) by preventing one of the first clock pulses from reaching the second clock circuitry (i.e. "to cause the divided to slip by one pulse of the serial clock on the line 26"; col. 3, lines 30-32). Buckland discloses that the serial input / parallel output shift register is the length of m-bits (fig. 1, ref. 16; col. 2, line 65). As broadly as claimed, each of Buckland's 8 bit search positions (see fig. 3) is considered to be a "frame". Therefore, the shift register has "at least as many stages as the number of bits of a frame" because it contains m bits (m is disclosed as 8 bits; col. 2, line 27) and m bits constitutes the length of a frame. As is conventionally understood, Buckland's 512 x 8 bits is considered a superframe. Finally, as broadly as claimed, Buckland's SLIP signal (see figure 1) "prevents one of the first clock pulses from

reaching the second clock circuitry" because it causes the second clock circuitry (fig. 1, ref. 20) to "slip by", overlook, or not act upon "one pulse of the serial clock".

Regarding claim 2, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that said controlling means is adapted so that the delay of the outputting of a frame is repeated several times until synchronization is reached (col. 2, lines 10-20).

Regarding claim 3, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that the frames have a fixed length of 8 bits as applied in claim 1 above.

Regarding claim 4, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that the frames are bytes (i.e. 8 bits each) as applied to claim 1 above.

Regarding claim 5, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses a first clock means (fig. 1, ref. 20) for generating first clock pulses (fig. 1, "CLOCK") clocking said parallel output portion (fig. 1, ref. 18) of said shift register means (fig. 1, refs. 16 and 18), wherein controlling means are adapted to control (via "SLIP" control; fig. 1) said first clock means so that said first clock pulses are delayed by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one (col. 3, lines 20-40).

Regarding claim 6, Buckland discloses the limitations of claim 5 as applied above. Further, Buckland discloses that each frame (including the frame word) includes N or m bits (i.e. "N" = "m"; fig. 1; col. 37-39), a second clock means (not shown) is

Art Unit: 2611

provided for generating second clock pulses (fig. 1, ref. 25) for clocking said serial input portion of said shift register means, and said first clock means (fig. 1, ref. 20) converts said second clock pulses into said first clock pulses (fig. 1, "CLOCK") having a time period which is N or m times (i.e. "N" – "m"; fig. 1, ref. 20, ( $\div$  m DIVIDER)) longer than the time period of said second clock pulses, characterized in that said controlling means is adapted to control said first clock means so that said first clock pulses are delayed by at least one time period of said second clock pulses (col. 3, lines 20-40).

Regarding claim 7, Buckland discloses the limitations of claim 5 as applied above. Further, Buckland discloses that said controlling means is adapted to supply a ("kick-pin") control signal (fig. 1, output of control circuit 10; "SLIP") to said first clock means (fig. 1, ref. 20), and said first clock means is adapted so that its output is modified by said control signal for at least one time period which is needed for shifting a bit in said serial input portion of said shift register means from a stage to a next one (col. 3, lines 20-40).

Regarding claim 8, Buckland discloses the limitations of the claim as applied to claim 1 above.

Regarding claim 9, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 2 above.

Regarding claim 10, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 11, Buckland discloses the limitations of claim 10 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 4 above.

Regarding claim 12, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

Regarding claim 13, Buckland discloses the limitations of claim 12 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

Regarding claim 14, Buckland discloses the limitations of claim 12 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckland in view of Giorgetta et al (U.S. Pat. No. 7035292; "Giorgetta").

Regarding claim 15, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that serial data is transported over a single channel (fig. 1, ref. 24) and, at the receiving side, is converted into parallel data (fig. 1, "m") for

Art Unit: 2611

further processing. Buckland does not disclose the use of the device in a digital data transmission systems like SONET/SDH or Gigabit Ethernet. However, systems like SONET/SDH or Gigabit Ethernet are well known in the art as suggested by Giorgetta (col. 3, lines 20-30). Further, Giorgetta discloses synchronizing to a frame (col. 7, lines 1-30). In view of the disclosure of Giorgetta, one skilled in the art would have recognized that the exemplary frame synchronization device of Buckland is capable of frame synchronization in SONET and Gigabit Ethernet applications. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the device of Buckland could be applied as a frame synchronization device in a SONET or Gigabit Ethernet application as suggested by Giorgetta because such applications require frame synchronization and are well known in the art.

***Allowable Subject Matter***

7. No claims are allowed.

***Conclusion***

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of



Art Unit: 2611

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/  
Art Unit 2611  
August 5, 2008

/Jmp/

Application/Control Number: 10/538,576

Page 9

Art Unit: 2611

/Chieh M Fan/  
Supervisory Patent Examiner, Art Unit 2611